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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,216	09/30/1998	RONALD PASQUALINI	NSC1-D8400	6392

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LAW OFFICES OF MARK C. PICKERING
P.O. BOX 300
PETALUMA, CA 94953

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/164,216	PASQUALINI, RONALD	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,19 and 38-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40-44* is/are allowed.

6)☒ Claim(s) *15,19,38,39,45-57,60-62,65 and 66* is/are rejected.

7)☒ Claim(s) *58,59,63 and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *38* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15, 19, 38-39, 45-57, 60-62 and 65-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. (5,515,225) considered alone, or over Gens et al. in view of Admitted Prior Art (APA).

Gens et al. teach in figure 3 and related text a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising a plurality of pads P1, P2, an ESD negative ring R2, a plurality of ESD positive lines (the horizontal lines located between the high power supply terminals (the square blocks indicated as VDD1 and VDD2) and the line connecting the two diodes. See also column 3, lines 32-49) not being directly connected to a steady voltage source, not being electrically connected to each other, not being directly connected to a pad, and not encircling the periphery of the chip; a plurality of switches (diodes) connected between the ESD positive lines and the ESD negative ring, and a plurality of first and

second diodes D1, D2 connected to a pad and the negative ring and positive line, respectively.

Although Gens et al. do not explicitly state that plurality of switches are connected between the ESD positive lines and the ESD negative ring, this feature is inherent in Gens et al.'s device, because it is well known in the art that diodes are switches, of which official notice is taken. Therefore, Gens et al. teach plurality of switches being connected between the ESD positive lines and the ESD negative ring, as claimed.

In the alternative, APA teaches in figures 1 and 2 and related text a plurality of ESD switches including a transistor (figure 2) connected to the positive line and to the negative ring, respectively (page 2, lines 24-27), wherein the transistor pass current from a positive line to a negative ring when a voltage on the positive line rises at a first rate.

It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to connect plurality of switches between the ESD positive lines and the ESD negative ring in Gens et al.'s device in order to provide more effective unidirectional flow of current during ESD operation.

Regarding claim 19, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claim 39, APA teaches in figure 2 a plurality of ESD switches including a transistor. It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to use a transistor as an ESD switch in Gens et al.'s device, because it is well known in the art to use a transistor as an ESD switch.

Regarding claim 46, Gens et al. teach in figure 3 a second diode having an anode electrically connected to a pad.

Regarding claim 51, APA teaches in figures 1 and 2 and related text a plurality of ESD switches including a transistor (figure 2) connected to the positive line and to the negative ring, respectively (page 2, lines 24-27), wherein the transistor pass current from a positive line to a negative ring when a voltage on the positive line rises at a first rate.

Regarding claim 52, Gens et al. teach in figure 3 switches (diodes) blocking a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

Regarding claim 53, Gens et al. teach in figure 3 second diodes forward biased when the voltage on the positive line rises at a second rate.

Regarding claims 54, 61 and 66, Gens et al. teach in figures 3 and 4 that none of the positive lines encircles the periphery of the chip.

Regarding claim 55, Gens et al. teach in figure 3 a positive line connected to a negative ring via a plurality of ESD switches.

Regarding claim 56, Gens et al. teach in figure 3 ESD switches (those connected to VDD1), not being connected to a pad P2.

Regarding claims 60 and 65, Gens et al. and APA teach ESD switches not being directly connected to a pad.

Regarding claims 57 and 62, Gens et al. teach in figure 3 only one second diode D1 is connected between a pad P2 and a positive line Vddi. Note that R1 is Vddi, a positive line (column 4, lines 7-8).

Allowable Subject Matter

3. Claims 40-44 are allowed.

4. Claims 58, 59, 63 and 64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 15 and 51 would be allowed if the phrase "each second diode is connected between a pad and a positive line." would read "only one second diode is connected between each pad and each positive line.". Claims 57 and 62 would be allowed if the phrase "only one second diode is connected between a pad and a positive line." would read "only one second diode is connected between each pad and each positive line."

Reasons for allowance

6. The following is an examiner's statement of reasons for allowance:
Gens et al. (5,515,225) appears to be the closest prior art reference. Gens et al. teach substantially the entire claimed structure as recited in claim 40, except disclosing the structure of the first diode. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant argues on pages 9 and 19 that positive lines of Gens et al. are directly connected to a pad, because voltage source Vdd1 is a pad.

Although Gens et al. name positive line Vdd1 as a voltage pad, Gens et al.'s structure is identical to the claimed structure by considering that the first and second diodes are connected to positive and negative voltages, wherein the I/O pad is connected in between the diodes and not being directly connected to a pad. Therefore, the positive lines of Gens et al. are not directly connected to a pad. Furthermore, claims are interpreted in light of the specification. When the specification provides definitions for terms appearing in the claims, the specification can be used in interpreting claim language. In re Vogel , 164 USPQ 619, 622 (CCPA 1970). The term "pad" is defined in the specification as an I/O pad and not as a supply voltage. Therefore, positive line Vdd1 can not be regarded as a "pad", as argued by applicant.

8. The rest of applicant's argument on page 11 with respect to claim 15 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant argues on page 12 that during a telephone interview, applicant's attorney understood that claims 15 and 51 would be allowed if amended to recite that only one second diode is connected between a pad and a positive line.

During a telephone interview on 12/13/2002, the examiner explained to applicant's attorney that there must have been some misunderstanding because Gens et al. teach the limitation of "only one second diode is connected between a pad and a positive line" since diode D1 is connected between pad P1 and positive line R1. The examiner further stated that the claims can be allowed if recited that "only one second diode is connected between each pad and each positive line."

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG

30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
December 15, 2002

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800